Analysis of Signal Integrity in High-Speed Digital IC's, by Combining MOSFET Modeling and the LE-FDTD Method

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Abstract— **For the reliable design of high-speed digital integrated circuits, signal integrity analysis of the critical interconnection lines need to be performed. Such an analysis should account for electromagnetic effects (propagation, impedance mismatch, cross-talk and substrate losses) as well as for the nonlinear behavior of the active circuitry. This work proposes a comprehensive approach to carry-out the above analysis. In particular, an accurate MOSFET analytical model, suitable for advanced submicrometric microelectronic technologies, has been incorporated in a full-wave simulator based on the Lumped Element Finite Difference Time Domain (LE-FDTD) method. In this abstract, discretization and implementation procedures are discussed, and some preliminary simulations, aimed at validating the approach, are presented.**

I. Introduction

THE reliable design of modern, digital, high-speed integrated circuits must account for propagation effects along the lines which interconnect digital gates [1]. Technology-scaling yields faster and smaller transistors , whereas interconnecting lines does not scale in a comparably favorable fashion [2]; on the contrary, since the die-area does not necessarily scale down, interconnections length may even increase, at least on an average basis. This makes the impact of signal ringing, clock skew, cross-talk and other propagation effects much more critical on advanced VLSI circuit design than it was for previous technology generations [3].

CAD tools have been devised, aimed at evaluating propagation effects and their influence on the circuit behavior: it is customary, to this respect, to identify a subset of critical signal paths (long or tightly-coupled nets), to be analyzed in detail by means of conventional circuit-analysis tools (e.g., SPICE). Within such a context, digital gates are described by comprehensive models of MOS transistors, whereas interconnection lines, responsible of propagation effects, are described by lumped-element equivalent circuits. The quality of the simulation results is therefore closely related to the reliability of such equivalent circuits: the definition of sensible circuit topologies and the characterization of their components represent a crucial bottleneck in the CAD design flow. Difficulties comes, in particular, from the inherently distributed nature of propagation effects, which scarcely lends itself to the rather drastic approximations (both physical and geometrical) usually implied in the formulation of equivalent-circuit SPICE models.

In this work, a different approach is proposed for the analysis of critical interconnection lines embedded into densely integrated circuits: here, electromagnetic field propagation is described on a distributed, physically-accurate basis, accounting at the same time for a sophisticated and comprehensive description of MOSFET devices. In particular, an advanced MOS model [4] (compatible with circuit simulation standards and thus sharing the same parameter set), is incorporated into a full-wave Maxwell equations solver, based on the Lumped Element Finite Difference Time Domain (LE-FDTD) method. The proposed approach hence allows for the rigorous modeling of electromagnetic effects (propagation, impedance mismatch, cross-talk, radiation and substrate losses), without the need of introducing approximated equivalent circuits, and carefully accounting for the nonlinear behavior of the digital circuits which terminate the nets.

II. Method

The self-consistent solution of device equations and of full-wave, field-propagation equations is made possible by the Lumped-Element, Finite Difference Time Domain algorithm [5]: basically, it consists of a strategy aimed at coupling time- and space-discretized Maxwell's equations with non-linear, equivalent circuits describing active devices. According to the LE-FDTD method, the device equivalent-circuit is "mapped" onto a few cells of the discretization mesh exploited for the numerical solution of field equations: in the following, such a process is applied to the advanced model of MOSFET devices developed at Philips and known as level 9.02 model.

The MOS transistor model is illustrated in Fig. 1(a): it consists of the voltage-controlled drain current source and of four non-linear capacitors. Drain- and source-bulk junctions are accounted for as well, and are not

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shown in figure, for the sake of clarity. Avalanche current, responsible for the drain-bulk breakdown is taken into account by the I_{AV} current source. A complete discussion of the interdependency among branch currents and node voltages and charges goes beyond the scope of this paper, and can be found in the model's reference documentation [6]: here it may be sufficient to mention that many second-order effects, typical of submicrometric devices (such as short- and narrow-channel effects, etc.), are accurately accounted for, resulting in a fairly complicated formulation of the device equations, which features over 80 parameters. Such parameters, in turn, can be extracted by experimental device characterization: by using, in the present context, a widely diffused SPICE-model, virtually compatible with standard circuit tools, we may rely, to this purpose, on the parameter sets usually distributed by silicon foundries. Despite its inherent intricacy, the model exhibits a simple topology, featuring a limited number of equivalent bipolar elements: each of these elements is associated to a different side of two contiguous FDTD cells.

As proposed by Sui *et al* [5], such a lumped element results in an additional current-density term $\mathbf{J}_\ell$, to be included into Ampere's equation:

$$\nabla \times \mathbf{H} = \epsilon_0 \frac{\partial \mathbf{E}}{\partial t} + \mathbf{J}_\ell \tag{1}$$

Mapping of the field components on the mesh cells, according to the Yee's notation [7], is illustrated in Fig. 1(b); for instance, assuming that the source terminal of the MOS transistor is connected to the node (i_s, j_s, k_s), the FDTD discretization procedure yields the following update equation, for the electric field at the GS branch:

$$\mathbf{E}_{\mathrm{GS}}^{n+1} = \mathbf{E}_{\mathrm{GS}}^{n} + \frac{\Delta t}{\epsilon_0} [\mathbf{u}_z \cdot \nabla \times \mathbf{H}]_{\mathbf{r}_{\mathrm{GS}}}^{n+\frac{1}{2}} - \frac{1}{\epsilon_0 \, \Delta x \, \Delta y} \left(Q_{\mathrm{GS}}^{n+1} - Q_{\mathrm{GS}}^{n} \right). \tag{2}$$

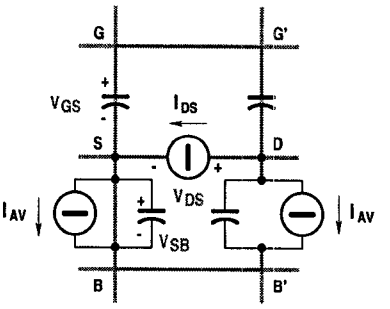
Here, $\mathbf{r}_{\mathrm{GS}} = \left(i_s, j_s, k_s + \frac{1}{2}\right)$ denotes the spatial position of $\mathbf{E}_{\mathrm{GS}}$, $\mathbf{u}_z$ the unit vector of the z axis and the expression of the discretized curl term is written in a compact form; more detailed expressions can be found in [7].

In the above equation, the charge Q_{GS} accumulated in the GS capacitor, depends, in a nonlinear fashion, on V_{GS}, V_{SB} and V_{DS} voltages. These, in turn, can be obtained by integrating the electric field over the corresponding edges; for instance:

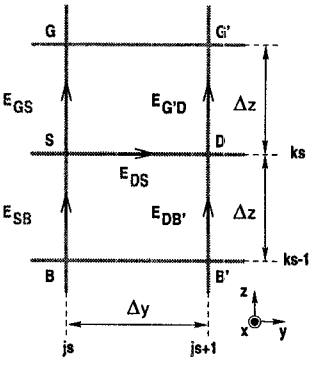
$$V_{\mathrm{GS}} = -\mathbf{E}_{\mathrm{GS}} \, \Delta z. \tag{3}$$

Inserting Eqs. (2) and (3) in (1) the following voltage update equation is thus obtained:

$$V_{\mathrm{GS}}^{n+1} = A_{\mathrm{GS}}^{n+\frac{1}{2}} +$$



(a) MOS transistor model



(b) FDTD mesh and variables

Fig. 1. FDTD compatible model of the MOS transistor. This model is composed by two voltage-controlled current generators and four nonlinear capacitors.

$$+\frac{1}{\epsilon_0} \frac{\Delta z}{\Delta x \, \Delta y} Q_{\mathrm{GS}} \left(V_{\mathrm{GS}}^{n+1}, V_{\mathrm{SB}}^{n+1}, V_{\mathrm{DS}}^{n+1} \right) \tag{4}$$

In the above equation, the voltages at the time step $n+1$ are unknown, while the term A_{GS} (which accounts for the memory of the system) is computed by using the variables computed at the previous time step:

$$A_{\mathrm{GS}}^{n+\frac{1}{2}} = -\frac{\Delta t \, \Delta z}{\epsilon_0} [\mathbf{u}_z \cdot \nabla \times \mathbf{H}]_{\mathbf{r}_{\mathrm{GS}}}^{n+\frac{1}{2}} - \frac{1}{\epsilon_0} \frac{\Delta z}{\Delta x \, \Delta y} Q_{\mathrm{GS}}^{n} + V_{\mathrm{GS}}^{n} \tag{5}$$

Similar procedures apply to the SB and DS branches, yielding:

$$V_{\mathrm{SB}}^{n+1} = A_{\mathrm{SB}}^{n+\frac{1}{2}} + \frac{1}{\epsilon_0} \frac{\Delta z}{\Delta x \, \Delta y} Q_{\mathrm{SB}} \left(V_{\mathrm{GS}}^{n+1}, V_{\mathrm{SB}}^{n+1}, V_{\mathrm{DS}}^{n+1} \right) \tag{6}$$

$$A_{\mathrm{SB}}^{n+\frac{1}{2}} = -\frac{\Delta t\,\Delta z}{\epsilon_0}\left[\mathbf{u}_z \cdot \nabla \times \mathbf{H}\right]_{\mathbf{r}_{\mathrm{SB}}}^{n+\frac{1}{2}} - \frac{1}{\epsilon_0}\frac{\Delta z}{\Delta x\,\Delta y} Q_{\mathrm{SB}}^{n} + V_{\mathrm{SB}}^{n} \quad (7)$$

and

$$V_{\mathrm{DS}}^{n+1} = A_{\mathrm{DS}}^{n+\frac{1}{2}} - \frac{1}{2\,\epsilon_0}\frac{\Delta t\,\Delta y}{\Delta x\,\Delta z} I_{\mathrm{DS}}\left(V_{\mathrm{GS}}^{n+1}, V_{\mathrm{SB}}^{n+1}, V_{\mathrm{DS}}^{n+1}\right) \quad (8)$$

$$A_{\mathrm{DS}}^{n+\frac{1}{2}} = -\frac{\Delta t\,\Delta y}{\epsilon_0}\left[\mathbf{u}_y \cdot \nabla \times \mathbf{H}\right]_{\mathbf{r}_{\mathrm{DS}}}^{n+\frac{1}{2}} - \frac{1}{2\,\epsilon_0}\frac{\Delta t\,\Delta y}{\Delta x\,\Delta z} I_{\mathrm{DS}}^{n} + V_{\mathrm{DS}}^{n} \quad (9)$$

for the DS branch. In Eqs. (4), (6) and (8), relationships between the quantities Q_{GS}, Q_{SB}, I_{DS} and the control voltages come from the Philips L9.02 model: updated voltages, in turn, are eventually used to evaluate the electric fields at the remaining cells. The resulting system of equations is solved, at each time step, by using an iterative (i.e., Newton-Raphson) algorithm: this implies a number of critical implementation issues, which cannot be exhaustively discussed in this paper, and include, to name just a few, the adaptive selection of the simulation time step, the monitoring of convergence and numerical stability, the efficient computation of the Jacobian matrix, and the control of "numerical" parasitic reactances, coming from unphysical coupling between lumped elements and field simulation domain.

III. Results

In order to validate the implementation of the MOSFET model in the LE-FDTD framework, a simple nMOS inverter has been considered, which is shown in the inset of Fig. 2. The whole circuit (including voltage sources and the load resistor) is described by lumped components, which, in turn, are embedded in a uniform FDTD mesh. The MOSFET features a 10 μm-wide and a 0.5 μm-long channel region; technology-dependent parameters are taken from a commercial CMOS 0.35 μm fabrication process; a 7 KΩ load is accounted for and a digital, rail-to-rail signal drives the gate, featuring 0.3 ns rise and fall times. Since no significant propagation domain is accounted for in this case, LE-FDTD results can be compared with those coming from more conventional, quasi-static circuit simulators: to this purpose, the commercial tool SPECTRE has been used, which incorporates the same MOSFET compact model: matching between FDTD results and the reference data is very close, thus validating the implementation.

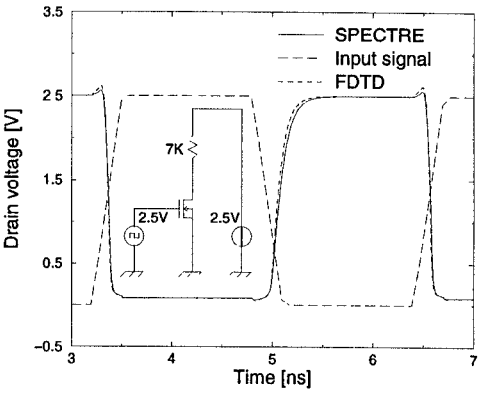


Fig. 2. FDTD simulated drain voltage for the simple inverter in the inset, compared with *SPECTRE* results.

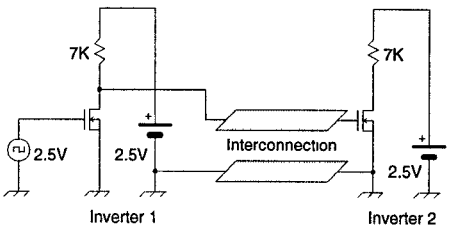


Fig. 3. Interconnection between two inverters.

A second, more significant test has been carried out on the circuit shown in Fig. 3: here, propagation along an ideal interconnection is accounted for. A wide metal net has been considered (which exhibits an almost negligible resistance), and increasing line lengths have been taken into account (thus increasing the capacitive load). Substrate losses are not accounted for, in this case, to make comparison with SPECTRE simulation easier. A couple of inverters, identical to the one described above, act as the line driver and receiver, respectively. Propagation times at the driver stage can be estimated by looking at Fig. 5.

Rising-edge propagation is much slower that falling-edge one: this is due to the different strengths of the (passive) pull-up and (active) pull-down networks on the inverter. As the line length increases, the t_{pLH} propagation time of the driver stage increases significantly, and the waveform suffers of severe degrade. The output signal at the receiver stage, instead, is shown in Fig. 4: the noise margins of the inverter are actually large enough to recover a full-swing output-signal.

Nevertheless, the propagation delay is clearly evident. In the same figure, comparison with SPECTRE output

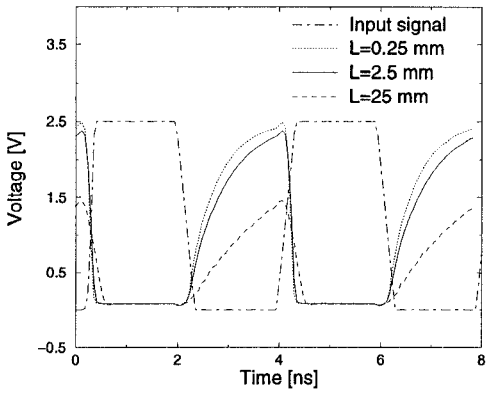


Fig. 4. Sensitivity to the line length for the output signal of inverter (1) of the circuit in Fig. 3.

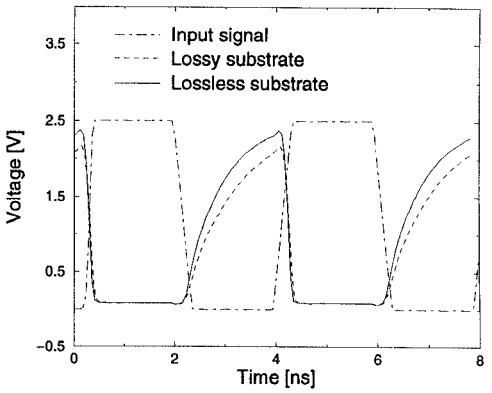


Fig. 6. FDTD simulation of the output signal of inverter (1), $L = 2.5\,\text{mm}$ in Fig. 3 considering the substrate losses.

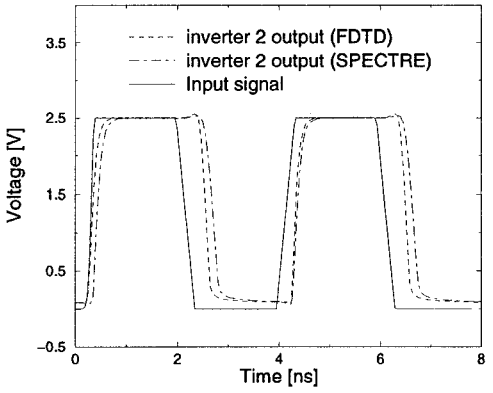


Fig. 5. FDTD simulation of the output signal of inverter (2), $L = 2.5\,\text{mm}$ in Fig. 3, compared with *SPECTRE* results

is given as well, still exhibiting a fair agreement; in the SPECTRE simulation, due to the large aspect ratio of the interconnect, the interconnect itself can be described by a bare capacitor. Finally, the same test structure has been simulated by refining the description of the physical interconnection: a SiO_2 layer is assumed as the dielectric, and a lossy ($\rho = 10^{-2}\,\Omega\cdot\text{cm}$) silicon substrate is accounted for. Simulation results for the lossy and the lossless substrate are compared in Fig. 6.

IV. Conclusions

A powerful simulation tool for the analysis of critical on-chip interconnections has been developed. It can self-consistently account for the nonlinear behavior of digital gates and for electromagnetic propagation effects along interconnections. Sophisticated models, suitable for the description of submicron MOSFET devices, have been incorporated into the code. Simple validation examples have been carried-out, to illustrate the method features and to validate the proposed approach. Nevertheless, it is worth emphasizing that the method does not impose, in principle, any restriction on the interconnect geometry, and can be straightforwardly applied to the analysis of a number of cases of practical interest, such as cross-talk analysis, identification of critical paths, etc. Since the distributed approach we follow to model the E.M. field propagation is inherently computationally expensive, our tool is not actually conceived for systematic, chip-level analysis: it is to be considered, instead, in a hierarchical framework, in which detailed results coming from LE-FDTD simulation are exploited for the accurate characterization of synthetic models, to be adopted, by analysis tools placed at a higher abstraction level.

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